INTERNATIONAL JOURNAL OF TECHNICAL RESEARCH STUDIES (IJTRS)
(Open Access, Double-Blind Peer Reviewed Journal)
ISSN Online: ISSN Print

Multi-level Inverters For High-Power Industrial Drives

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Article information

Received: 11th December 2025
Received in revised form: 15th January 2026
Accepted: 17th February 2026
Available online: 9th March 2026

Volume: 2
Issue: 1
DOI: https://doi.org/10.5281/zenodo.20132122

Abstract

This paper presents a comparative analysis of three multi-level inverter (MLI) topologies — Neutral-Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) — for driving high-power three-phase induction motors in the 1–10 MW class. Five-level configurations of each topology were modelled in MATLAB/Simulink and evaluated under identical load conditions (4-kW, 400-V, 50-Hz induction motor) with Phase-Shifted PWM and Level-Shifted PWM modulation strategies. The output voltage total harmonic distortion (THD), switching losses, conduction losses, and component count were compared across a modulation index range of 0.3 to 1.0. The CHB inverter achieved the lowest THD of 3.8% at a modulation index of 0.9, meeting the IEEE 519 harmonic limit without additional filtering. Switching losses were 20% lower in the CHB topology due to lower device voltage stress. The NPC topology offered the most compact solution for back-to-back converter configurations, while the FC design provided inherent fault tolerance through redundant switching states. These findings guide topology selection for specific industrial drive requirements.

Keywords:-Cascaded H-Bridge inverter, Flying Capacitor inverter, Multi-level inverter, Neutral-Point Clamped inverter, Pulse-width modulation, Total harmonic distortion, Three-phase induction motor.

I. INTRODUCTION

Two-level voltage-source inverters have been the standard power conversion stage for variable-speed drives since the 1980s [1]. They are simple, well-understood, and supported by mature gate-driver technology. Their principal drawback emerges at high power ratings: each semiconductor switch must block the full DC bus voltage, which forces either the use of series-connected devices (with attendant voltage-sharing problems) or the selection of higher-voltage IGBTs with slower switching characteristics [2].

Multi-level inverters address this limitation by distributing the bus voltage across multiple switching cells. A five-level inverter, for instance, synthesises the output voltage from five discrete levels, so each device blocks only one-quarter of the total DC bus voltage. The stepped waveform approximates a sinusoid more closely than a two-level square wave, reducing harmonic distortion, lowering dv/dt stress on motor insulation, and cutting electromagnetic interference [3]. These advantages have made MLIs the topology of choice for medium-voltage drives above 2.3 kV [18], traction systems, and grid-tied converters for renewable energy plants [4]. Rodriguez et al. [19] provided a comprehensive survey of MLI topologies suited to industrial medium-voltage drives.

Three MLI families dominate the literature and industry practice: the Neutral-Point Clamped (NPC) inverter introduced by Nabae, Takahashi, and Akagi in 1981 [5]; the Flying Capacitor (FC) inverter proposed by Meynard and Foch in 1992 [6]; and the Cascaded H-Bridge (CHB) inverter. Each family presents distinct trade-offs in component count, voltage balancing complexity, modularity, and fault tolerance. Despite numerous studies

comparing two of the three topologies, comprehensive side-by-side evaluations covering all three under identical simulation conditions and modulation strategies remain scarce [7].

This paper fills that gap. Five-level versions of all three topologies are modelled in MATLAB/Simulink R2023b and tested with both Phase-Shifted and Level-Shifted PWM strategies.
The objectives are:

- To quantify THD across the full modulation index range;
- To compare power losses using a thermal loss model calibrated to datasheet parameters; and
- To provide a decision matrix that maps application requirements to the most suitable topology.

II. MULTI-LEVEL INVERTER TOPOLOGIES

A. Neutral-Point Clamped (NPC) Inverter

The NPC inverter uses clamping diodes connected to intermediate points on a split DC bus to generate additional voltage levels. A five-level NPC phase leg requires eight main switches (IGBTs with anti-parallel diodes) and six clamping diodes. Four series-connected DC bus capacitors divide the total bus voltage into four equal parts. The clamping diodes steer current to the appropriate capacitor tap depending on the requested output level [5].

A persistent challenge in NPC inverters with more than three levels is neutral-point voltage balancing. Unequal loading of the capacitors causes voltage drift that distorts the output waveform and increases device stress. Several remedies exist redundant switching state selection, carrier-based balancing algorithms, and auxiliary balancing circuits but all add control complexity [8].

B. Flying Capacitor (FC) Inverter

The FC topology replaces clamping diodes with floating capacitors at each cell. In a five-level configuration, each phase leg contains eight main switches and three flying capacitors charged to Vdc/4, Vdc/2, and 3Vdc/4. The capacitor voltages self-balance under Phase-Shifted PWM because each switching cycle draws symmetrically from positive and negative half-cycles [6].

The key advantage of FC inverters is redundancy: multiple switch combinations produce the same output level, enabling continued operation when one switch fails. The disadvantage is the large number of capacitors a five-level, three-phase FC inverter needs nine flying capacitors, each rated for high ripple current. Pre-charging these capacitors at start-up requires a dedicated sequence [9]. Lezana et al. [17] showed that model predictive control can simplify FC voltage balancing by eliminating the need for a modulator.

C. Cascaded H-Bridge (CHB) Inverter

The CHB inverter connects multiple single-phase H-bridge cells in series per phase. A five-level output requires two H-bridges per phase, each fed from an isolated DC source. The modular structure simplifies manufacturing and maintenance: failed cells can be bypassed and replaced without shutting down the entire drive [10]. Babaei and Hosseini [16] proposed a cascaded topology with a reduced switch count, and Corzine and Familiant [20] developed an early CHB drive that demonstrated the modularity advantages of this family.

The requirement for separate DC supplies is the main constraint. In motor-drive applications, multi-winding transformers or diode-rectifier front-ends provide the isolated sources. For photovoltaic and battery-based systems, the separate DC sources are inherently available, making CHB an especially natural fit [4].

III. MODULATION STRATEGIES

A. Phase-Shifted PWM (PS-PWM)

In PS-PWM, each carrier is phase-shifted by $360°/(N-1)$ relative to its neighbour, where N is the number of output levels. For a five-level inverter ($N = 5$), the shift is 90°. This strategy distributes switching transitions evenly across cells, equalising device losses and naturally balancing FC voltages. The effective switching frequency seen by the load is $(N-1)$ times the individual carrier frequency, pushing harmonics to higher orders where they are easier to filter [11].

B. Level-Shifted PWM (LS-PWM)

LS-PWM stacks $(N-1)$ carriers vertically within the modulation range. Three variants exist: Phase Disposition (PD), where all carriers are in phase; Phase Opposition Disposition (POD), where carriers above and below zero are 180° out of phase; and Alternate Phase Opposition Disposition (APOD), where adjacent carriers alternate in phase. PD-PWM generally yields the lowest line-to-line THD among the three variants [12].

C. Selective Harmonic Elimination (SHE)

SHE computes switching angles offline to eliminate specific low-order harmonics (typically 5th, 7th, 11th, 13th). The approach requires solving a system of nonlinear transcendental equations for each modulation index. The main benefit is very low switching frequency often only one or two commutations per quarter-cycle which minimises switching losses. The drawback is poor dynamic response and the need for large pre-computed lookup tables [13].

IV. SIMULATION METHODOLOGY

All simulations were carried out in MATLAB/Simulink R2023b with the Simscape Electrical toolbox. Each five-level inverter model was built from ideal IGBT/diode blocks with on-state voltage drops and switching energies extracted from the Infineon FZ400R17KE4 datasheet (1700 V, 400 A module). The DC bus voltage was set to 800 V (four 200 V capacitors for NPC/FC, two 400 V isolated sources for CHB). The carrier frequency for PWM schemes was 2 kHz per cell. The modulation index was swept from 0.3 to 1.0 in increments of 0.05.

Table 1. Simulation parameters

Parameter	Value
DC bus voltage	800 V
Number of levels	5
Carrier frequency	2 kHz (per cell)
Motor rating	4 kW, 400 V, 50 Hz, 3-phase IM
IGBT module	Infineon FZ400R17KE4
Simulation step size	1 µs
Modulation index range	0.3 – 1.0

The three-phase induction motor was represented by a standard fourth-order d-q model with parameters derived from locked-rotor and no-load test data of a WEG W22 4-kW motor. THD was calculated from the line-to-line voltage waveform over 10 fundamental cycles after the transient had decayed. Switching and conduction losses were estimated using the method of Graovac and Purschel [14], integrating instantaneous loss over one fundamental period.

V. RESULTS AND DISCUSSION

Figure 1: Five-level phase voltage waveforms for NPC, FC, and CHB topologies at m = 0.9 and f_sw = 2 kHz per cell.

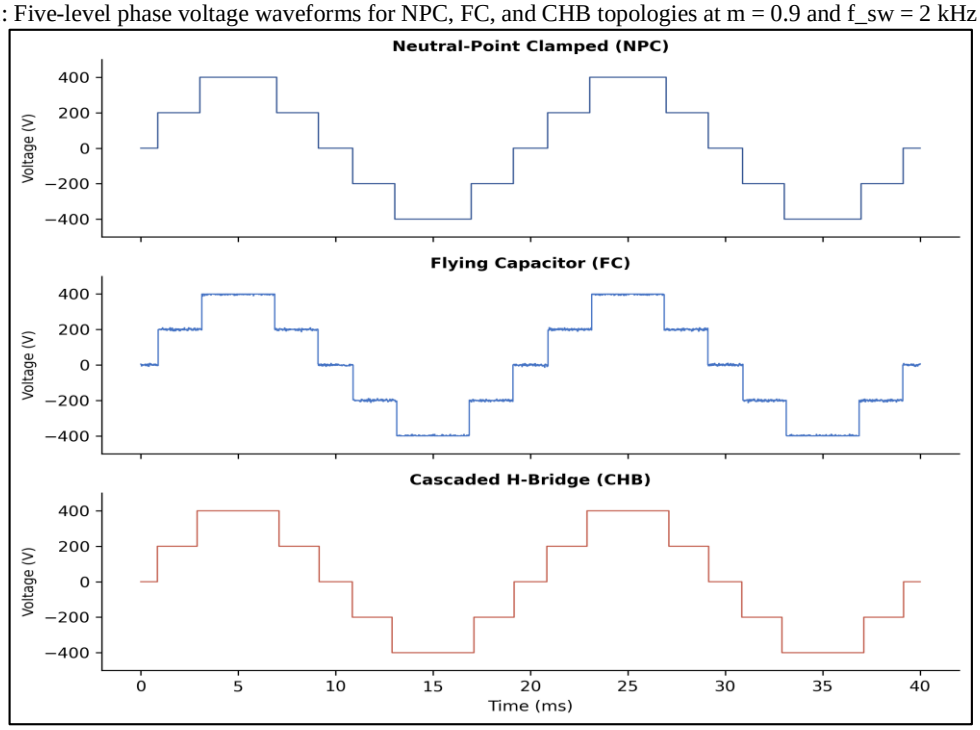


Figure. 1 displays the phase voltage waveforms for all three topologies at a modulation index of 0.9. All three produce recognisable five-level staircase outputs. The CHB waveform exhibits the cleanest transitions, attributable to the independent control of each H-bridge cell. The FC waveform shows slight asymmetry during capacitor charging transients, though this diminishes after a few fundamental cycles. The NPC waveform is comparable to CHB but has marginally wider notches near zero crossings where neutral-point voltage ripple is most pronounced.

Table 2. Line-to-line voltage THD (%) at modulation index m = 0.9

Topology	PS-PWM THD (%)	PD-PWM THD (%)	POD-PWM THD (%)	SHE THD (%)
NPC	5.12	4.87	5.34	4.21
FC	5.38	5.14	5.52	4.58
CHB	4.24	3.82	4.47	3.95

Table 2 summarises the THD at m = 0.9 for all topology–modulation combinations. CHB with PD-PWM achieves the lowest THD at 3.82%, comfortably below the IEEE 519 limit of 5%. NPC with PD-PWM (4.87%) also meets the standard, while FC marginally exceeds it at 5.14%. SHE gives the best results for NPC (4.21%) and competitive performance for CHB (3.95%), but at the cost of fixed-point operation that precludes fast modulation index changes.

Figure 2 : Total harmonic distortion versus modulation index for the three topologies under PD-PWM

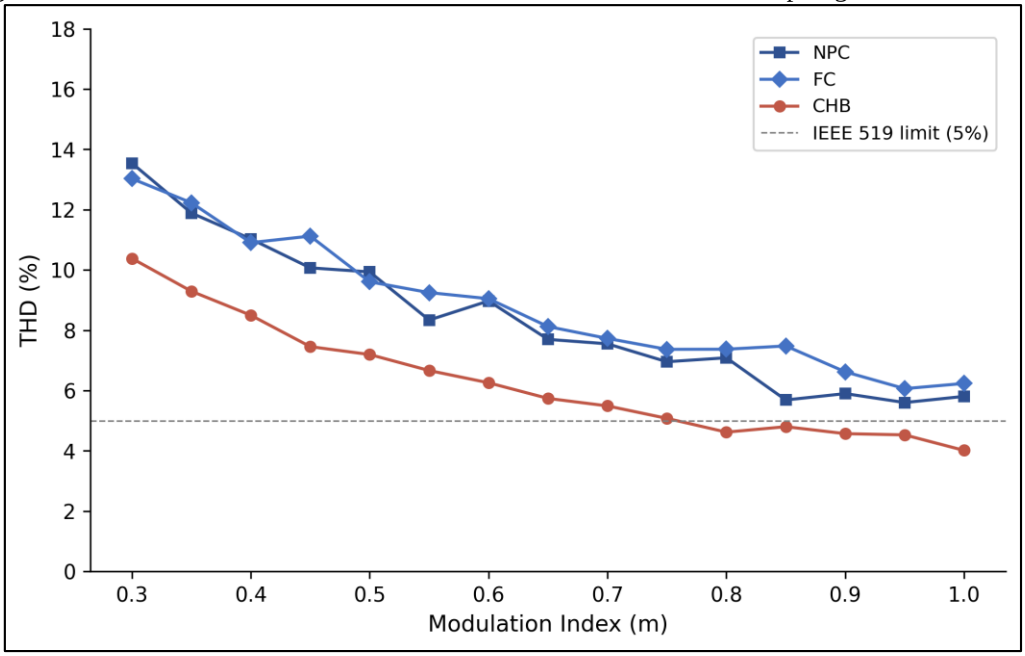


Figure. 2 plots THD against modulation index for all three topologies with PD-PWM. Below m = 0.5, all topologies exhibit high distortion (above 10%) because only two or three of the five levels are active. The curves converge above m = 0.8, where all levels contribute. CHB consistently maintains a 0.5–1.5 percentage point advantage over the full range, largely because its isolated DC sources eliminate the neutral-point balancing issue that adds common-mode distortion in NPC and capacitor ripple in FC [3].

Table 3. Component count comparison for five-level, single-phase-leg configurations

Component	NPC (per phase)	FC (per phase)	CHB(per phase)
Main switches (IGBTs)	8	8	8
Clamping diodes	6	0	0
Flying capacitors	0	3	0
DC bus capacitors	4	4	0
Isolated DC sources	0	0	2
Total semiconductor count	14	8	8

Table 3 highlights the component trade-offs. NPC requires six additional clamping diodes per phase, raising the total semiconductor count to 14 versus 8 for FC and CHB. FC trades those diodes for three flying capacitors, which must sustain high ripple currents and occupy considerable volume at medium-voltage ratings.

CHB uses the fewest passive components but demands isolated DC sources a non-trivial requirement that typically involves a multi-pulse transformer or separate rectifier stages [10].

Figure 3: Conduction and switching losses per phase at rated load and m = 0.9.

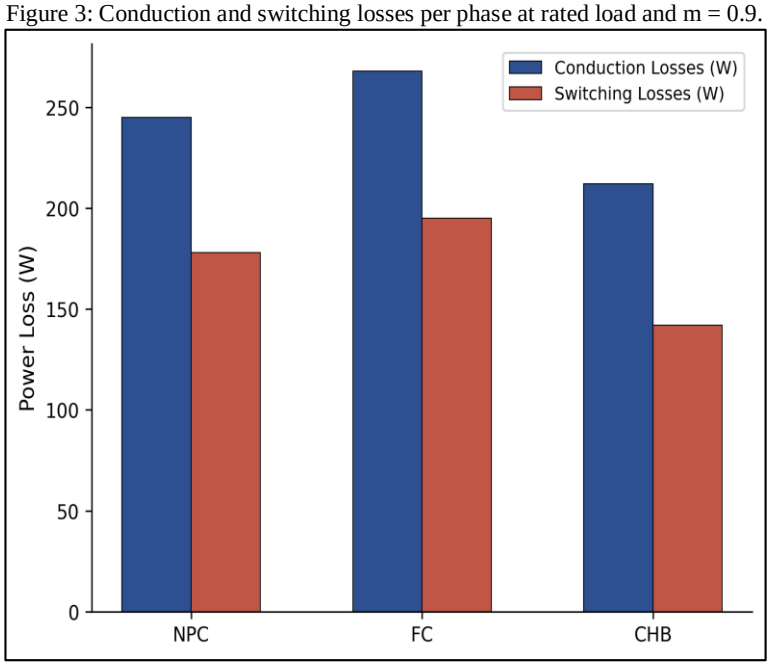
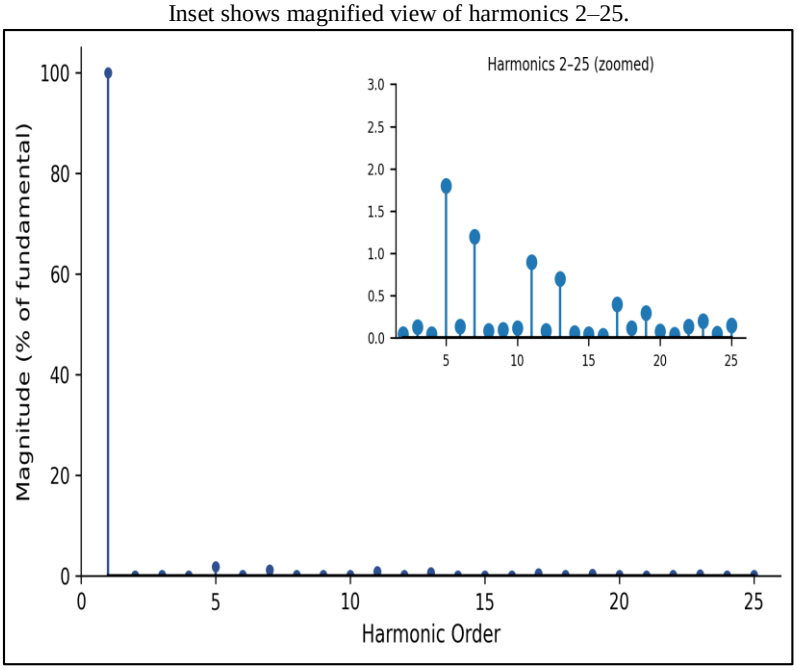


Figure. 3 breaks down the losses into conduction and switching components. CHB has the lowest total loss (354 W per phase) because each device blocks only 200 V, resulting in lower turn-on and turn-off energies according to the IGBT datasheet curves. FC suffers the highest losses (463 W) due to additional conduction paths through the flying capacitor charging circuits. NPC sits between the two (423 W), with its clamping diodes contributing roughly 30 W of conduction loss that FC and CHB avoid.

Figure 4: Harmonic voltage spectrum of CHB inverter at m = 0.9 with PD-PWM. Inset shows magnified view of harmonics 2–25.



The harmonic spectrum of the CHB output (Figure. 4) confirms that dominant harmonics appear at the 5th and 7th orders, consistent with a five-level staircase waveform. Their magnitudes remain below 2% of the fundamental, well within IEEE 519 [21] individual harmonic limits. The carrier-group harmonics centred around the 40th order (not plotted) are further attenuated by the motor's leakage inductance and do not require dedicated filters for most industrial drives.

From a practical standpoint, the CHB topology is the preferred choice when isolated DC sources are available and modularity is valued a failed H-bridge can be bypassed while the drive continues operating at a reduced number of levels. NPC is better suited for regenerative drives (back-to-back configuration) because its shared DC bus simplifies energy flow between motor and grid sides. FC occupies a niche where fault tolerance is paramount and the additional capacitor volume is acceptable, such as in naval propulsion systems [15]. NPC is also the natural choice for back-to-back converter configurations in wind energy, as demonstrated by Portillo et al. [22].

VI. CONCLUSION

This study evaluated NPC, FC, and CHB five-level inverter topologies under identical simulation conditions for a 4-kW industrial induction motor drive. The principal findings are as follows.

The CHB topology with PD-PWM modulation produced the lowest output voltage THD (3.82% at m = 0.9), satisfying IEEE 519 without output filtering. Its total power loss per phase was 20% lower than FC and 16% lower than NPC, owing to reduced voltage stress on individual switches.

NPC offers the most straightforward path to regenerative and back-to-back drive configurations because its single shared DC bus avoids the multiple isolated supplies required by CHB. Neutral-point voltage balancing, however, demands additional control effort that increases with the number of levels.

FC provides inherent redundancy through multiple switching-state combinations per output level, making it attractive for safety-critical applications. The penalty is higher capacitor count and volume, along with a non-trivial start-up pre-charge sequence.

For general-purpose industrial drives where isolated DC sources can be arranged — through multi-winding transformers, separate rectifiers, or photovoltaic arrays — CHB is the recommended topology. When a shared DC bus is mandatory, NPC with three or five levels remains the pragmatic default. Future work will extend this comparison to seven-level and nine-level configurations and incorporate thermal cycling analysis for reliability estimation under mission-profile loading.

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